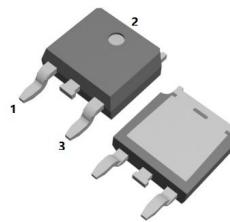
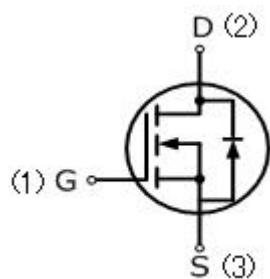


## 5N65(G,D)S

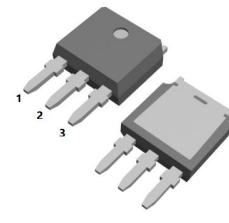
5 Amps, 650 Volts N-Channel Super Junction Power MOSFET

### FEATURE

- 5A, 650V,  $R_{DS(ON)MAX}=1.0\ \Omega$  @  $V_{GS}=10V/2A$
- Low gate charge
- Low  $C_{iss}$
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



TO-252-2L  
5N65GS



TO-251-3L  
5N65DS

### Absolute Maximum Ratings ( $T_c=25^\circ C$ , unless otherwise noted)

Parameter	Symbol	5N65(G,D)S	UNIT
Drain-Source Voltage	$V_{DSS}$	650	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current	$I_D$	5	A
Pulsed Drain Current (Note 1)	$I_{DM}$	15	
Single Pulse Avalanche Energy (Note 2)	$E_{AS}$	61	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	°C
Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	$T_L$	260	°C

### Thermal Characteristics

Parameter	Symbol	5N65(G,D)S	Units
Maximum Junction-to-Case	$R_{thJC}$	3.41	°C/W
Maximum Power Dissipation	$T_c=25^\circ C$	37	W

Electrical Characteristics ( $T_c=25^\circ\text{C}$ , unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$\text{BV}_{\text{DSS}}$	$\text{V}_{\text{GS}}=0\text{V}, \text{I}_D=250\text{uA}, T_c=25^\circ\text{C}$	650	—	—	V
Zero Gate Voltage Drain Current	$\text{I}_{\text{DSS}}$	$\text{V}_{\text{DS}}=650\text{V}, \text{V}_{\text{GS}}=0\text{V}$	—	—	1	$\mu\text{A}$
Gate-Body Leakage Current, Forward	$\text{I}_{\text{GSSF}}$	$\text{V}_{\text{GS}}=20\text{V}, \text{V}_{\text{DS}}=0\text{V}$	—	—	100	nA
Gate-Body Leakage Current, Reverse	$\text{I}_{\text{GSSR}}$	$\text{V}_{\text{GS}}=-20\text{V}, \text{V}_{\text{DS}}=0\text{V}$	—	—	-100	nA
<b>On Characteristics</b>						
Gate-Source Threshold Voltage	$\text{V}_{\text{GS(th)}}$	$\text{V}_{\text{DS}}=\text{V}_{\text{GS}}, \text{I}_D=250\text{uA}$	2.0	—	4.0	V
Drain-Source On-State Resistance	$\text{R}_{\text{DS(on)}}$	$\text{V}_{\text{GS}}=10\text{V}, \text{I}_D=2\text{A}$	—	0.87	1.0	$\Omega$
<b>Dynamic Characteristics</b>						
Input Capacitance	$\text{C}_{\text{iss}}$	$\text{V}_{\text{DS}}=25\text{V}, \text{V}_{\text{GS}}=0\text{V}, f=1.0\text{MHz}$	—	260	—	pF
Output Capacitance	$\text{C}_{\text{oss}}$		—	30	—	pF
Reverse Transfer Capacitance	$\text{C}_{\text{rss}}$		—	27	—	pF
<b>Switching Characteristics</b>						
Turn-On Delay Time	$t_{\text{d(on)}}$	$\text{V}_{\text{DD}}=325\text{V}, \text{I}_D=5\text{A}, R_G=10\Omega$	—	288.8	—	ns
Turn-On Rise Time	$t_r$		—	1	—	ns
Turn-Off Delay Time	$t_{\text{d(off)}}$		—	15.4	—	ns
Turn-Off Fall Time	$t_f$		—	5.8	—	ns
Total Gate Charge	$Q_g$	$\text{V}_{\text{DS}}=520\text{V}, \text{I}_D=5\text{A}, V_{\text{GS}}=10\text{V}$	—	10.5	—	nC
Gate-Source Charge	$Q_{gs}$		—	3.5	—	nC
Gate-Drain Charge	$Q_{gd}$		—	2.9	—	nC
<b>Drain-Source Body Diode Characteristics and Maximum Ratings</b>						
Diode Forward Voltage	$\text{V}_{\text{SD}}$	$I_S=2.5\text{A}, \text{V}_{\text{GS}}=0\text{V}$	—	—	1.3	V
Reverse Recovery Time	$t_{rr}$	$\text{V}_{\text{GS}}=0\text{V}, I_S=1\text{A}, dI_F/dt=50\text{A/us}$ (Note 3)	—	110	—	ns
Reverse Recovery Charge	$Q_{rr}$		—	501	—	nC

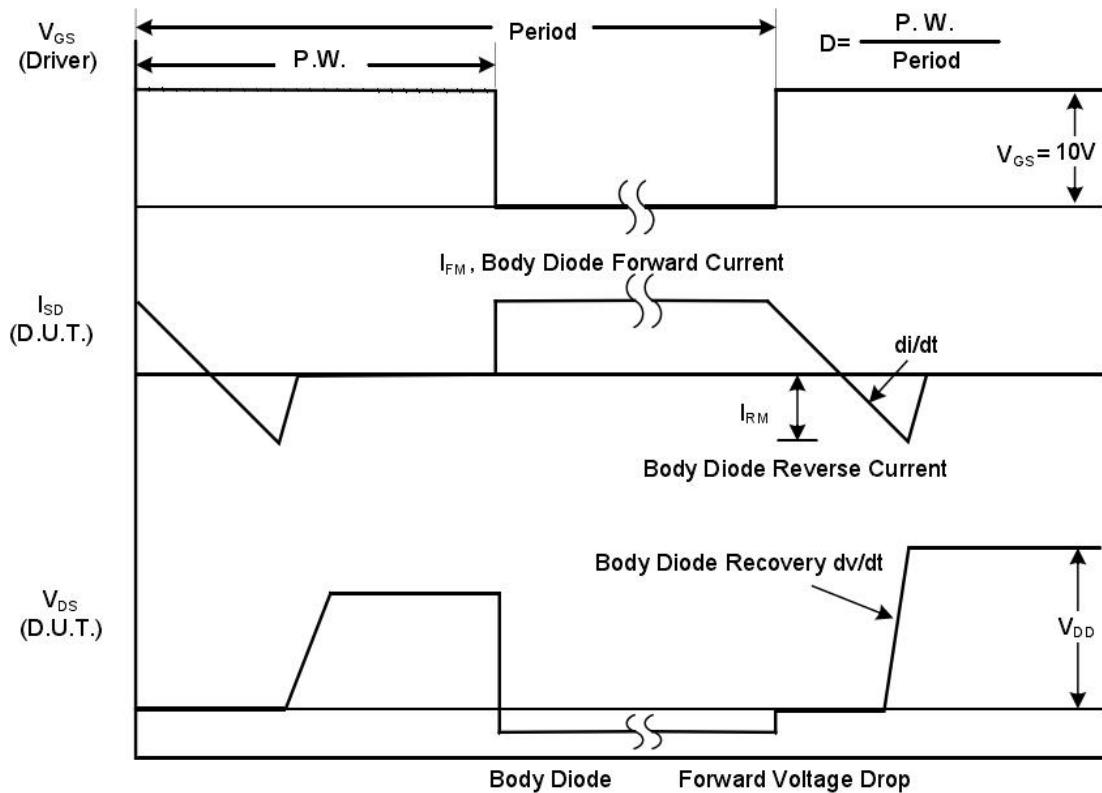
### Notes

1. Repetitive Rating:pulse width limited by maximum junction temperature.
2.  $L=10\text{mH}, R_g=25\Omega, V_{\text{DD}}=50\text{V}$ , starting  $T_j=25^\circ\text{C}$ .
3. Pulse width  $\leq 300\text{us}$ ; duty cycle  $\leq 2\%$ .

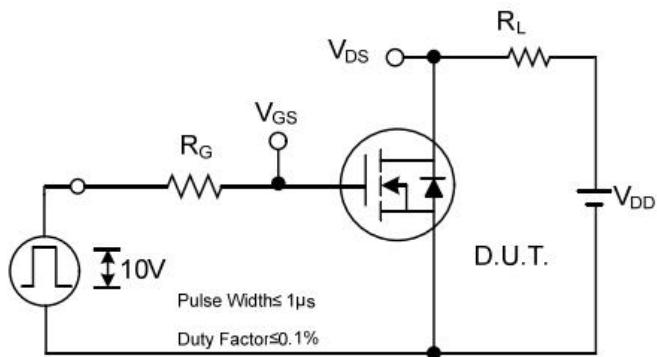
## RATING AND CHARACTERISTIC CURVES



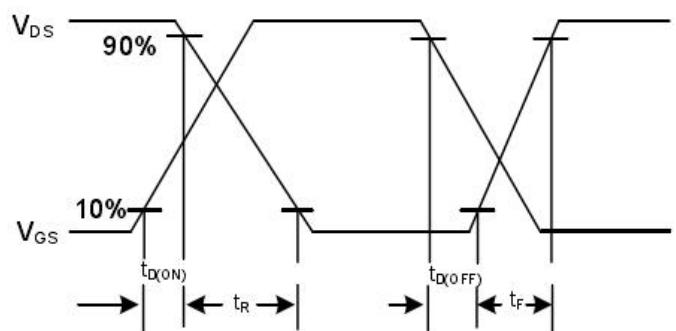
Peak Diode Recovery dv/dt Test Circuit



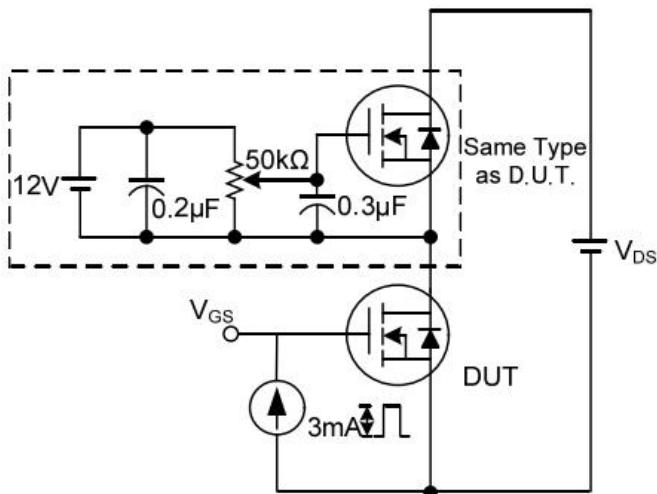
Peak Diode Recovery dv/dt Waveforms



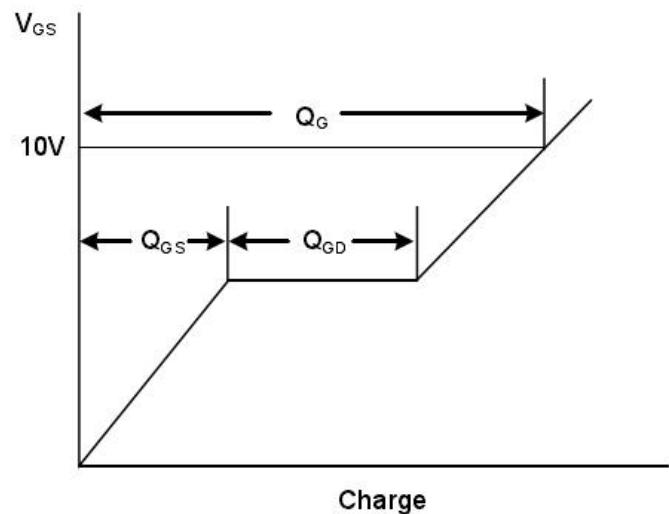
Switching Test Circuit



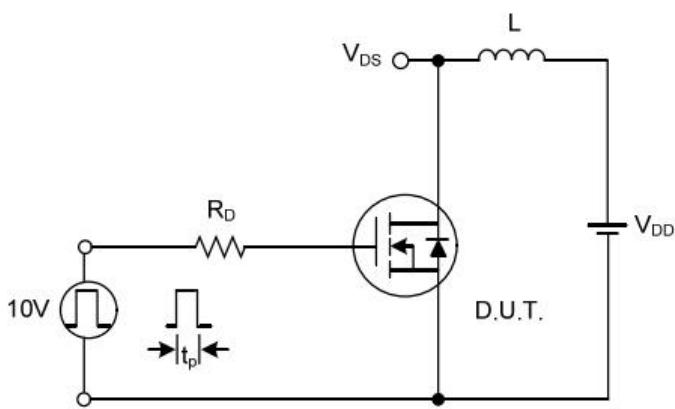
Switching Waveforms



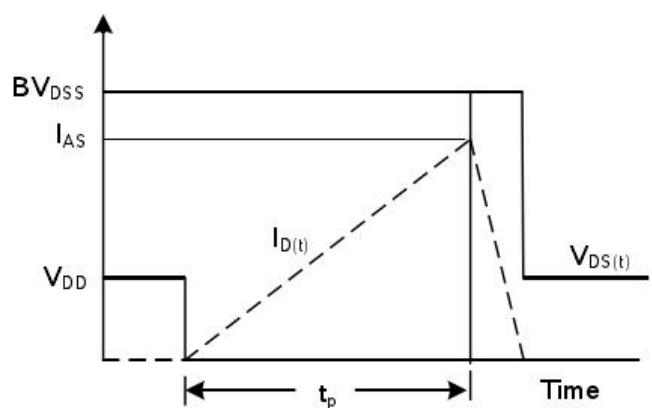
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

## RATING AND CHARACTERISTIC CURVES

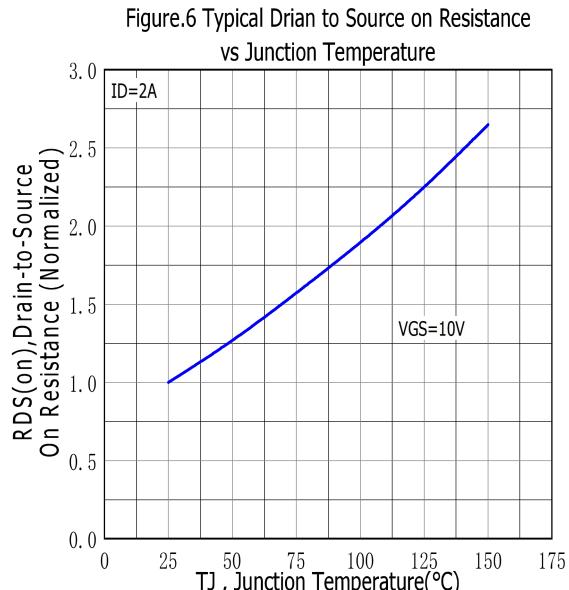
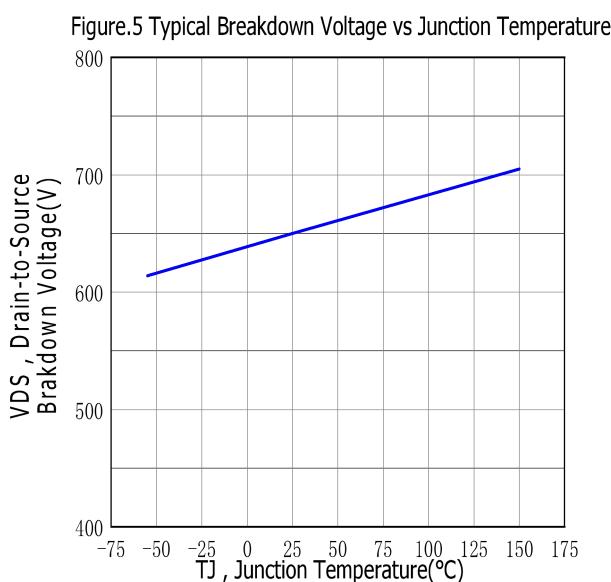
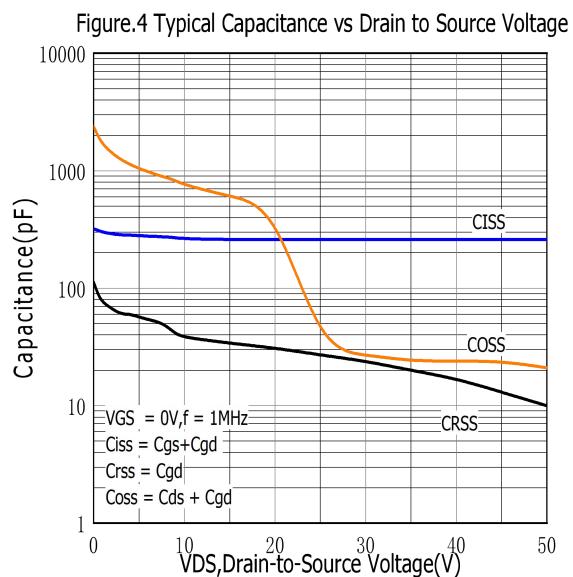
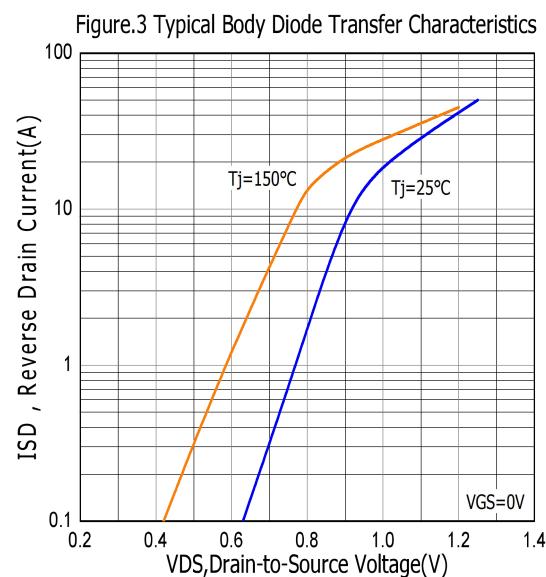
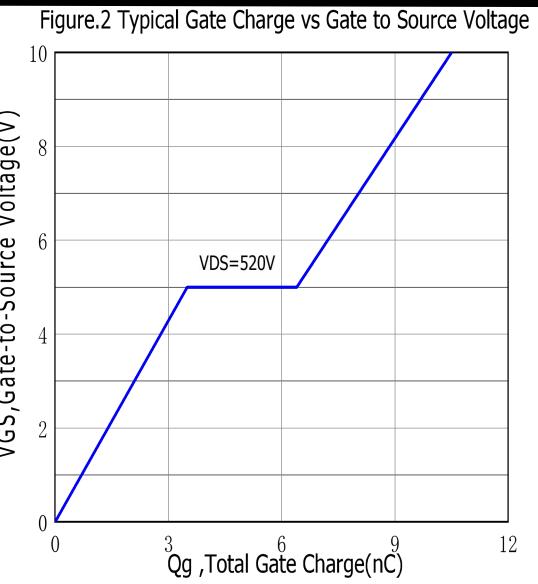
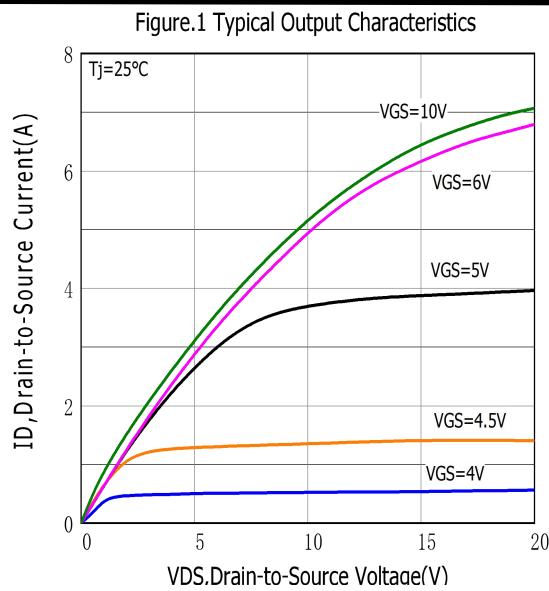


Figure.7 Maximum Forward Bias Safe Operating Area

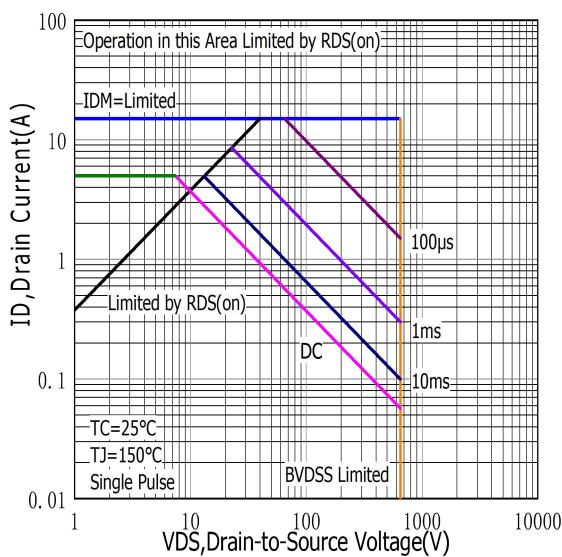


Figure.8 Typical Drain to Source ON Resistance vs Drain Current

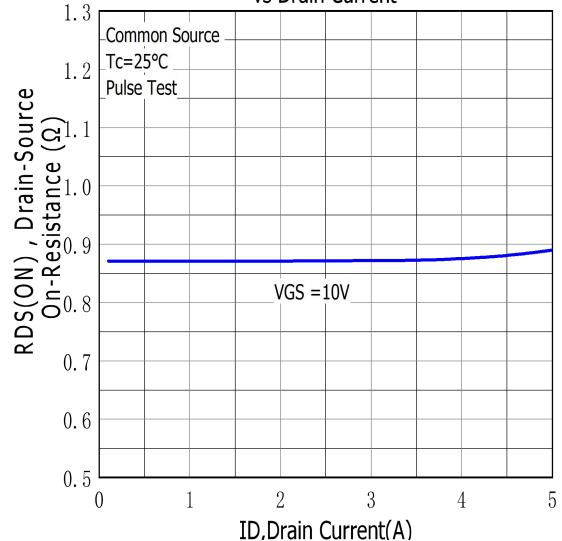


Figure.9 Maximum EAS vs Channel Temperature

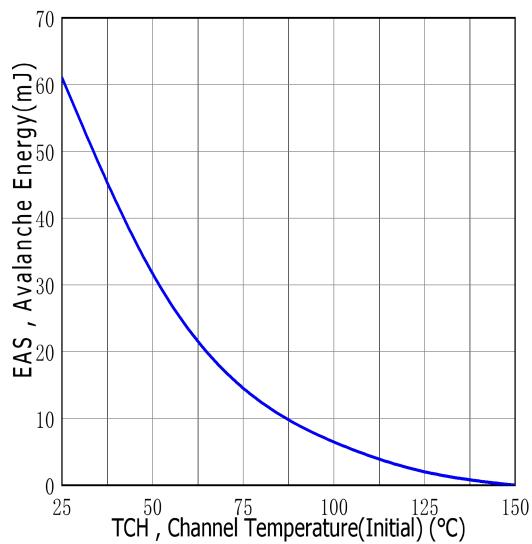


Figure.10 Typical Threshold Voltage vs Case Temperature

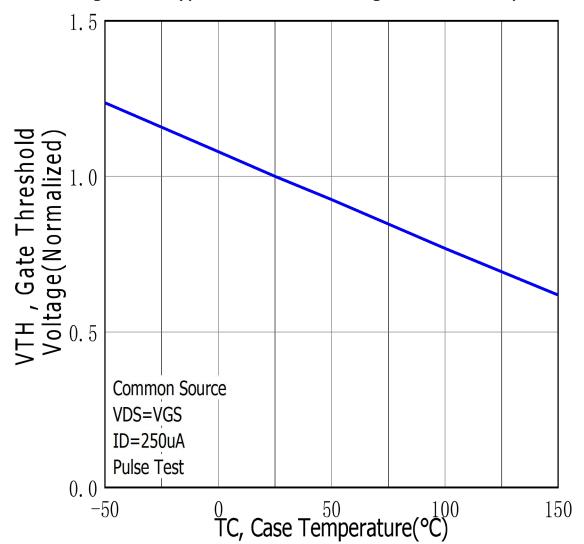


Figure.11 Maximum Effective Thermal Impedance , Junction to Case

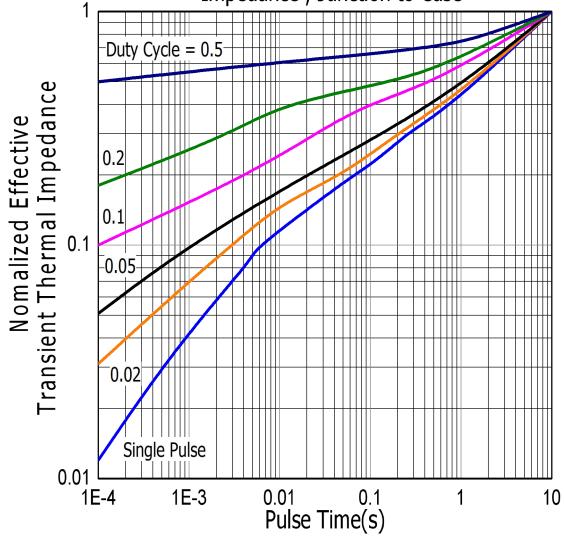
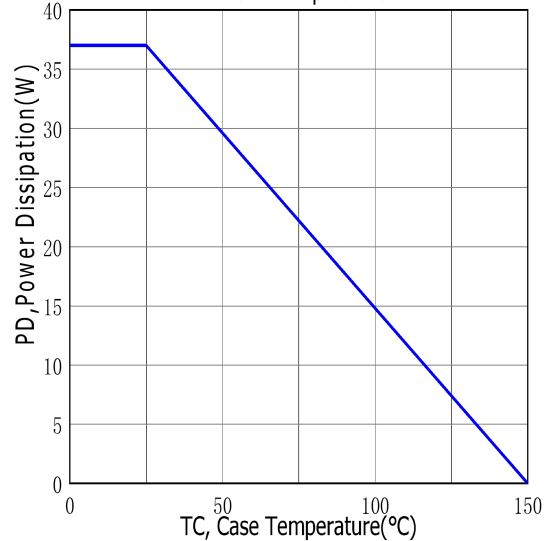
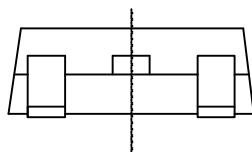
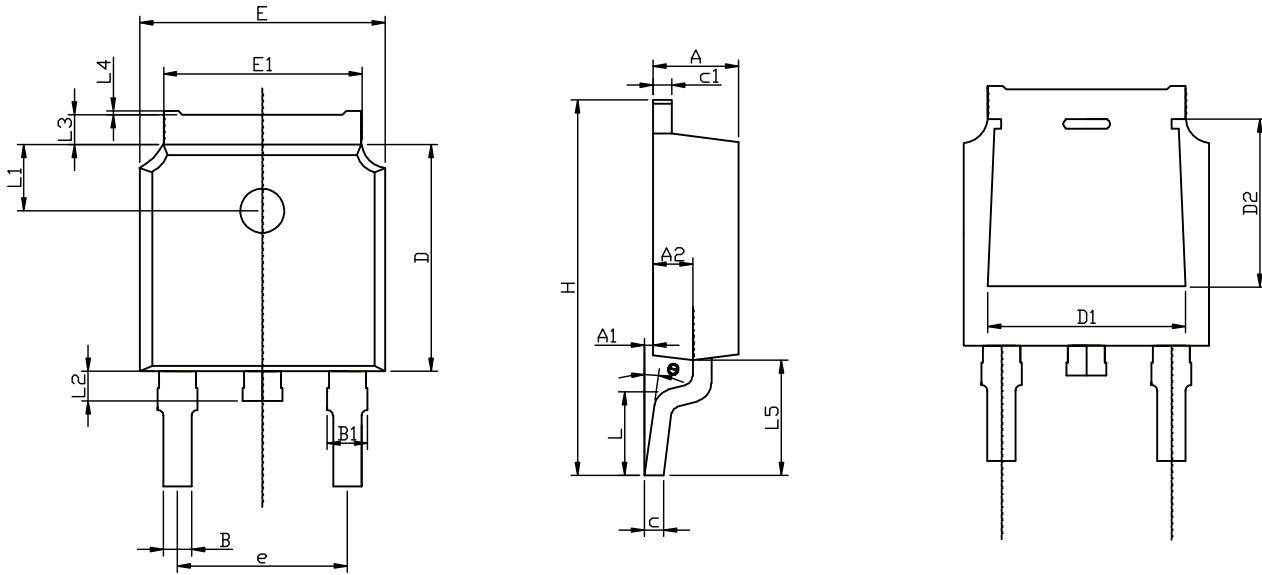


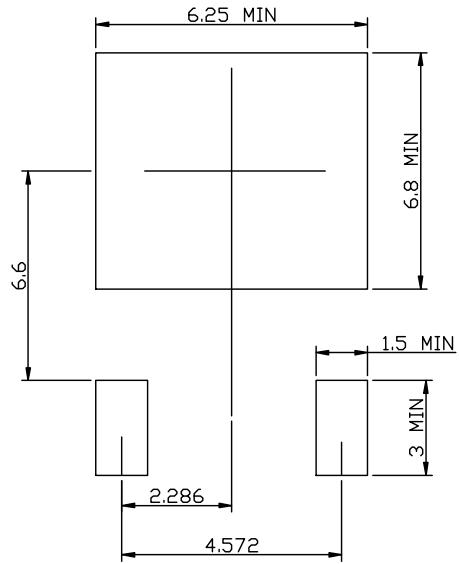
Figure.12 Maximum Power Dissipation vs Case Temperature



## TO-252-2L PACKAGE OUTLINE



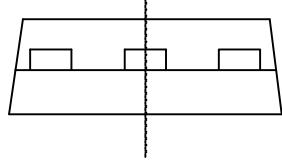
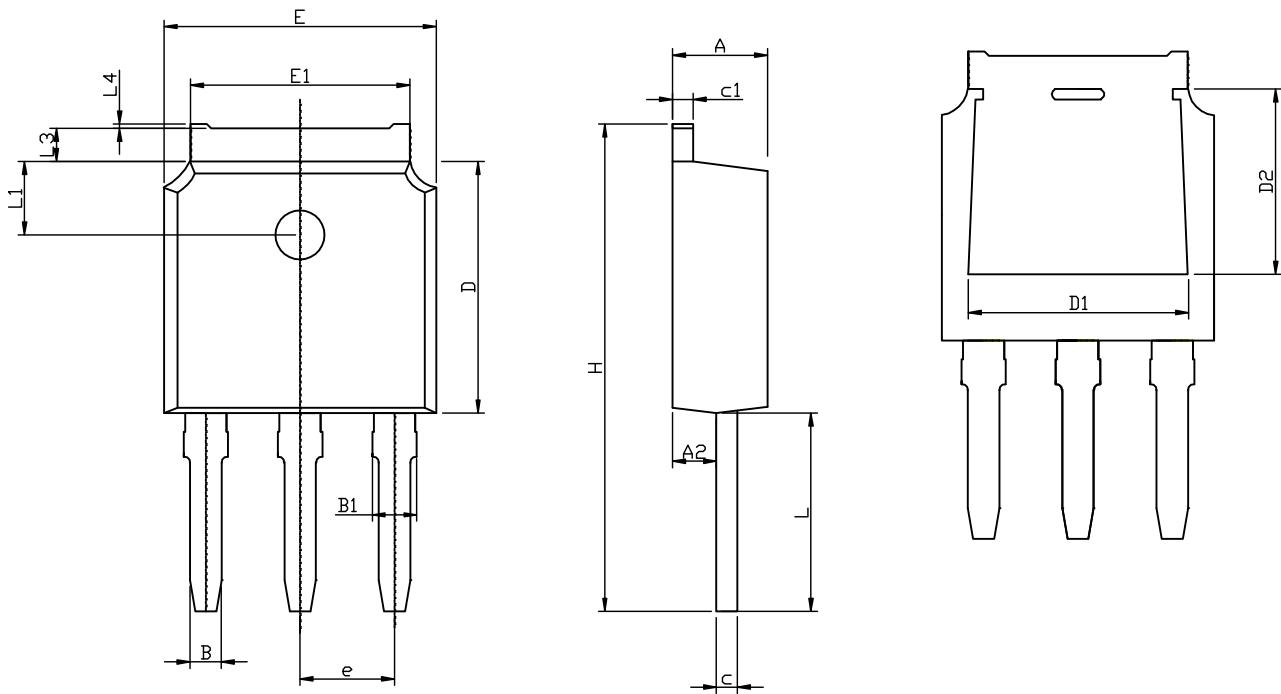
RECOMMENDED LAND PATTERN



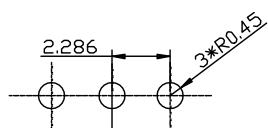
	MIN	NOM	MAX
A	2.15	2.30	2.45
A1	0.05	0.10	0.20
A2	0.91	1.07	1.22
B	0.66	0.76	0.86
B1	0.93	1.08	1.23
C	0.40	0.50	0.60
C1	0.40	0.50	0.60
D	5.95	6.10	6.25
D1	—	4.8REF	—
D2	—	3.8REF	—
E	6.45	6.60	6.75
E1	5.12	5.32	5.52
L		1.65	
L1	1.58	1.78	1.98
L2	0.60	0.80	1.00
L3	0.70	0.85	1.00
L4	0.00	0.05	0.20
L5	2.80	3.10	3.40
H	9.80	10.10	10.40
$\Theta$	0°		8°
e		4.572REF	

UNIT: mm

## TO-251-3L PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



UNIT: mm

	MIN	NOM	MAX
A	2.15	2.30	2.45
A2	0.91	1.07	1.22
B	0.66	0.76	0.86
B1	0.93	1.08	1.23
C	0.40	0.50	0.60
C1	0.40	0.50	0.60
D	5.95	6.10	6.25
D1	—	4.8REF	—
D2	—	3.8REF	—
E	6.45	6.60	6.75
E1	5.12	5.32	5.52
L	4.50	4.80	5.10
L1	1.58	1.78	1.98
L3	0.70	0.85	1.00
L4	0.00	0.05	0.20
H	11.50	11.80	12.10
e		2.286REF	